GSS4501

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	28mΩ
	I_D	7A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	50mΩ
	I_D	-5.3A

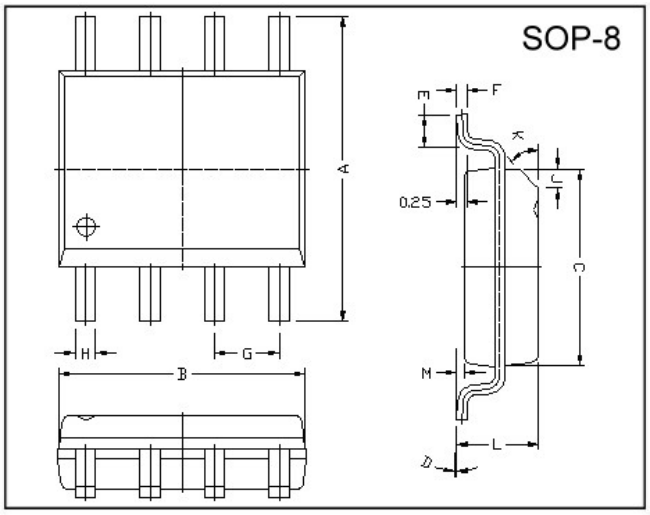
Description

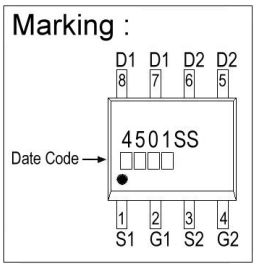
The GSS4501 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

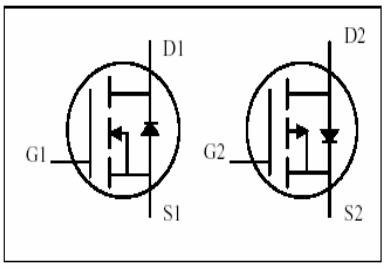
Features

*Simple Drive Requirement
*Lower On-resistance
*Fast Switching

Package Dimensions







REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-channel	P-channel	
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±16	V
Continuous Drain Current[3]	I_D @T_A=25℃	7	-5.3	A
Continuous Drain Current[3]	I_D @T_A=70℃	5.8	-4.7	A
Pulsed Drain Current[1]	I_{DM}	20	-20	A
Total Power Dissipation	P_D @T_A=25℃	2.0		W
Linear Derating Factor		0.016		W/℃
Operating Junction and Storage Temperature Range	Tj, Tstg	-55 ~ +150		℃

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient[3] Max.	Rthj-a	62.5	℃/W

N-Channel Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250uA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle Tj$	-	0.02	-	V/℃	Reference to 25℃, I_D=1mA
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transconductance	g_{fs}	-	13	-	S	V_{DS}=10V, I_D=7A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current(Tj=25℃)	I_{DSS}	-	-	1	uA	V_{DS}=30V, V_{GS}=0
Drain-Source Leakage Current(Tj=70℃)		-	-	25	uA	V_{DS}=24V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	28	mΩ	V_{GS}=10V, I_D=7A
		-	-	42		V_{GS}=4.5V, I_D=5A
Total Gate Charge[2]	Q_g	-	8.4	-	nC	I_D=7A V_{DS}=24V V_{GS}=4.5V
Gate-Source Charge	Q_{gs}	-	2.1	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	4.7	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	6	-	ns	V_{DS}=15V I_D=1A V_{GS}=10V R_G=3.3Ω R_D=15Ω
Rise Time	T_r	-	5.2	-		
Turn-off Delay Time	$T_{d(off)}$	-	18.8	-		
Fall Time	T_f	-	4.4	-		
Input Capacitance	C_{iss}	-	645	-	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
Output Capacitance	C_{oss}	-	150	-		
Reverse Transfer Capacitance	C_{rss}	-	95	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage[2]	V_{SD}	-	-	1.2	V	I_S=7A, V_{GS}=0V, Tj=25℃
Continuous Source Current (Body Diode)	I_S	-	-	1.67	A	V_D=V_G=0V, V_S=1.2V

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width≦300us, duty cycle≦2%.

3. Surface mounted on 1 in^2 copper pad of FR4 board; 135℃/W when mounted on Min. copper pad.

P-Channel Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D=-250uA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle Tj$	-	-0.028	-	V/℃	Reference to 25℃, I_D=-1mA
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	-	-3.0	V	V_{DS}=V_{GS}, I_D=-250uA
Forward Transconductance	g_{fs}	-	8.5	-	S	V_{DS}=-10V, I_D=-5.3A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±16V
Drain-Source Leakage Current(Tj=25℃)	I_{DSS}	-	-	-1	uA	V_{DS}=-30V, V_{GS}=0
Drain-Source Leakage Current(Tj=70℃)		-	-	-25	uA	V_{DS}=-24V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	50	mΩ	V_{GS}=-10V, I_D=-5.3A
		-	-	90		V_{GS}=-4.5V, I_D=-4.2A
Total Gate Charge[2]	Q_g	-	20	-	nC	I_D=-5.3A V_{DS}=-15V V_{GS}=-10V
Gate-Source Charge	Q_{gs}	-	3.5	-		
Gate-Drain ("Miller") Change	Q_{gd}	-	2	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	12	-	ns	V_{DS}=-15V I_D=-1A V_{GS}=-10V R_G=6Ω R_D=15Ω
Rise Time	T_r	-	20	-		
Turn-off Delay Time	$T_{d(off)}$	-	45	-		
Fall Time	T_f	-	27	-		
Input Capacitance	C_{iss}	-	790	-	pF	V_{GS}=0V V_{DS}=-15V f=1.0MHz
Output Capacitance	C_{oss}	-	440	-		
Reverse Transfer Capacitance	C_{rss}	-	120	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage[2]	V_{SD}	-	-	-1.2	V	I_S=-2.6A, V_{GS}=0V, Tj=25℃
Continuous Source Current (Body Diode)	I_S	-	-	-1.67	A	V_D=V_G=0V, V_S=-1.2V

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width≦300us, duty cycle≦2%.

3. Surface mounted on 1 in^2 copper pad of FR4 board; 135℃/W when mounted on Min. copper pad.

Characteristics Curve N-Channel

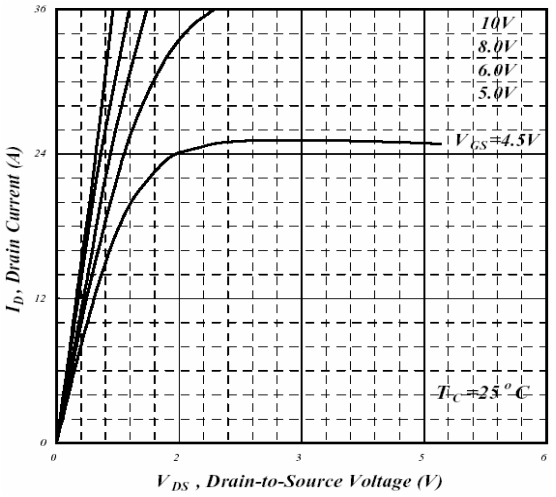


Fig 1. Typical Output Characteristics

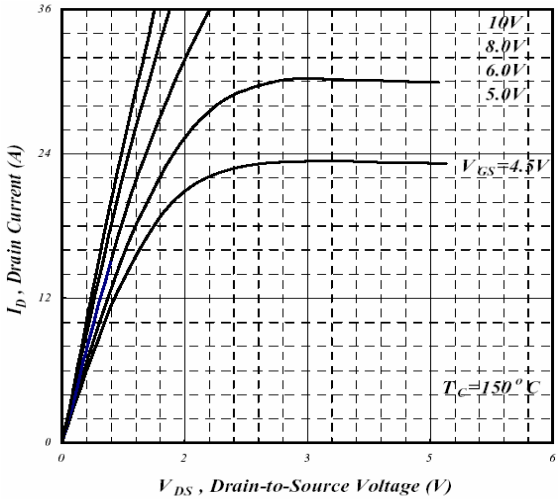


Fig 2. Typical Output Characteristics

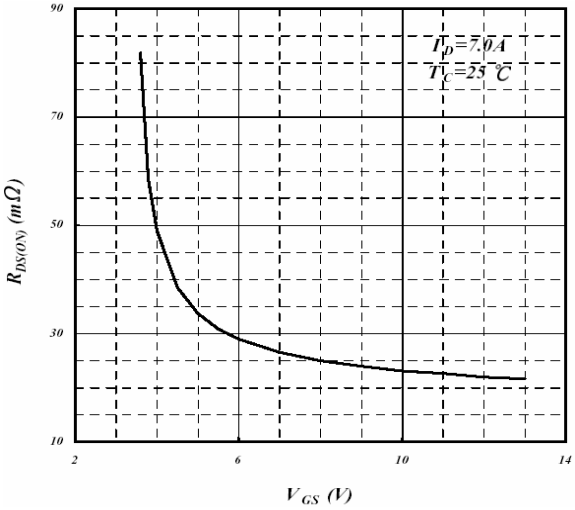


Fig 3. On-Resistance v.s. Gate Voltage

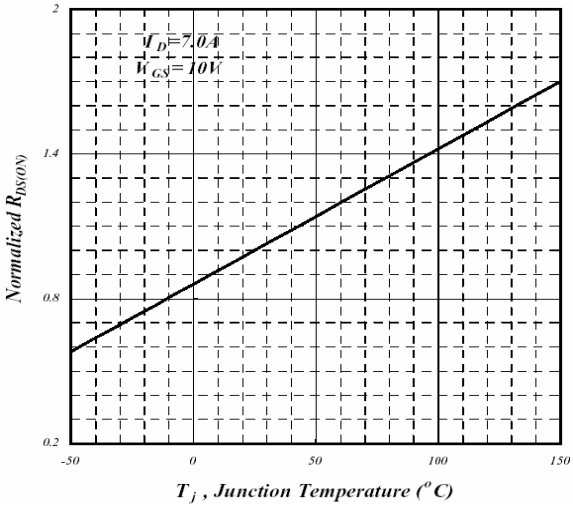


Fig 4. Normalized On-Resistance v.s. Junction Temperature

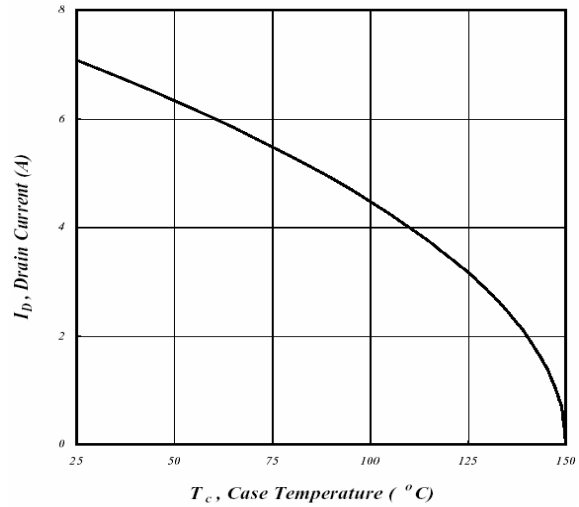


Fig 5. Maximum Drain Current v.s. Case Temperature

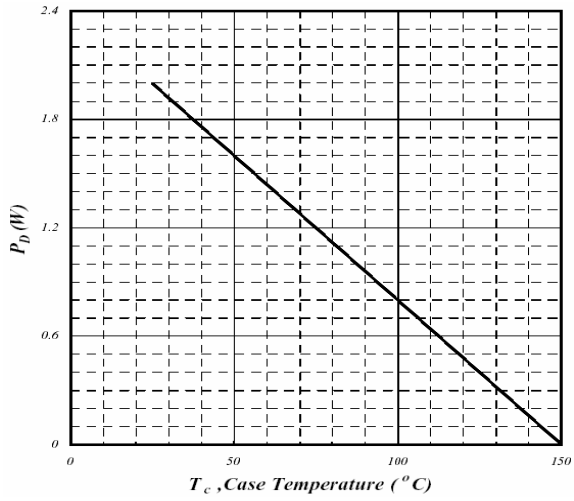


Fig 6. Type Power Dissipation

N-Channel

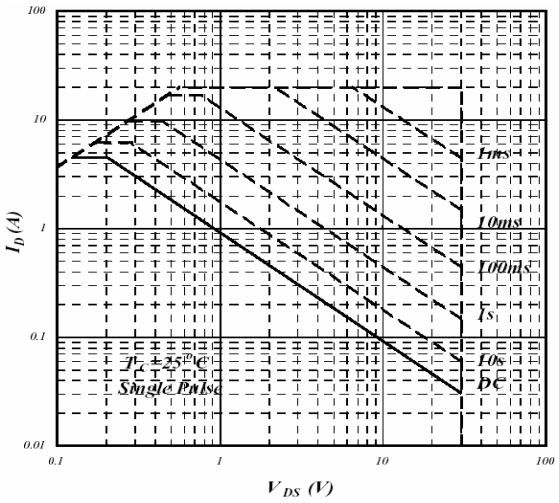


Fig 7. Maximum Safe Operating Area

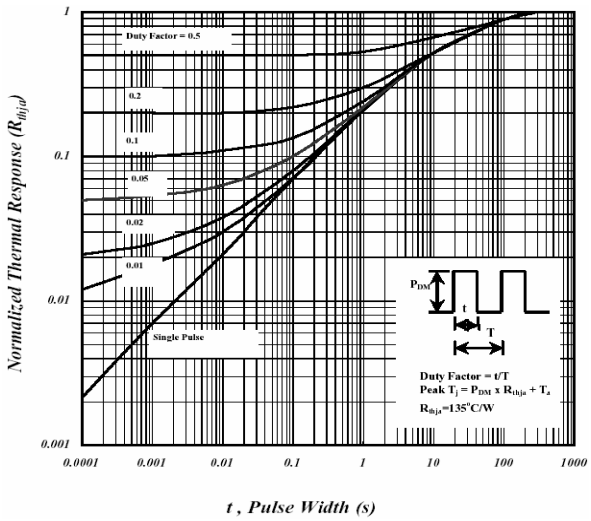


Fig 8. Effective Transient Thermal Impedance

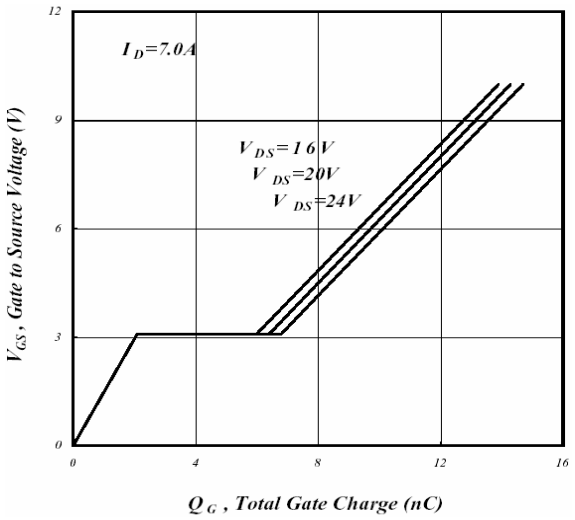


Fig 9. Gate Charge Characteristics

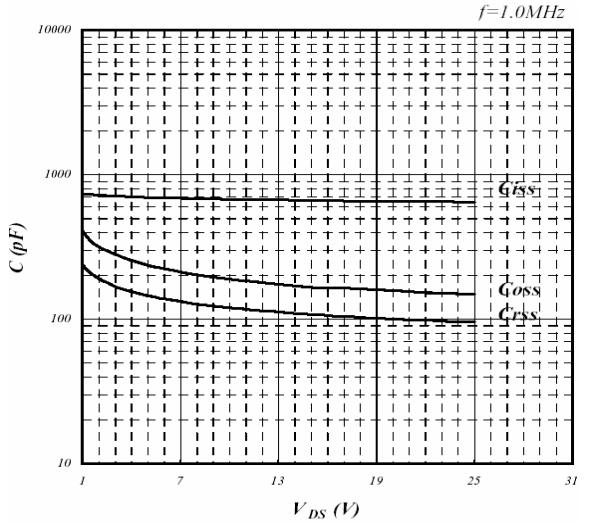


Fig 10. Typical Capacitance Characteristics

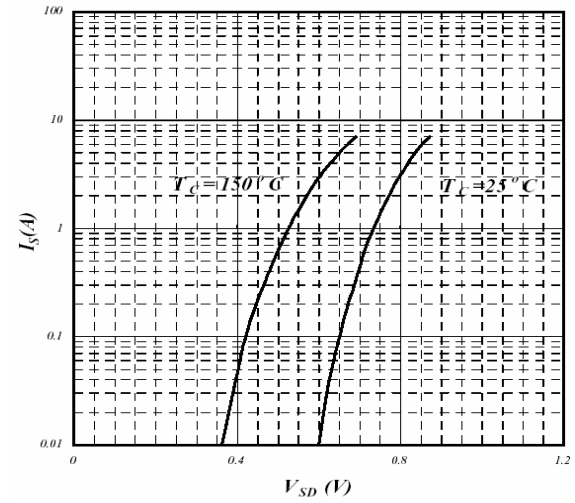


Fig 11. Forward Characteristics of Reverse Diode

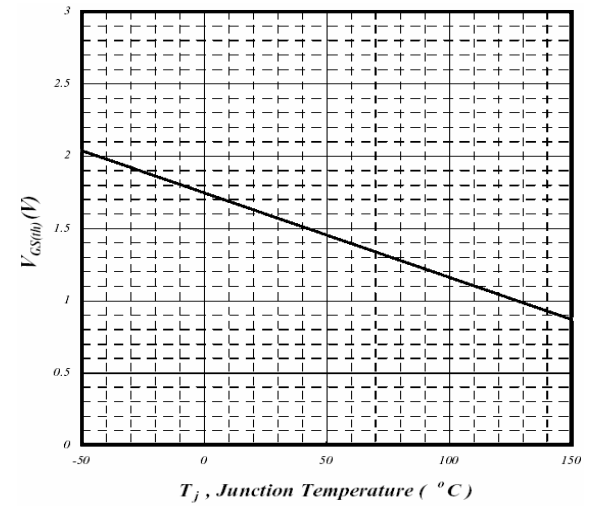


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

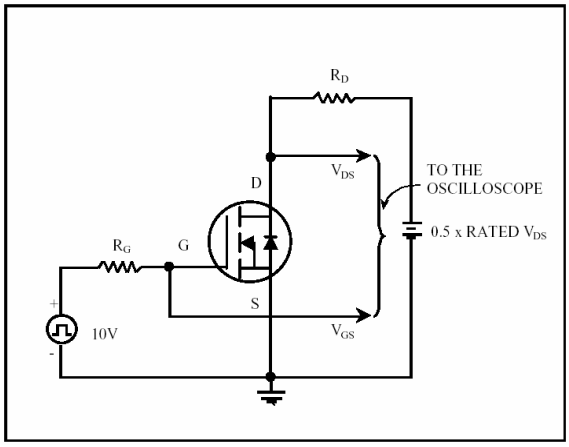


Fig 13. Switching Time Circuit

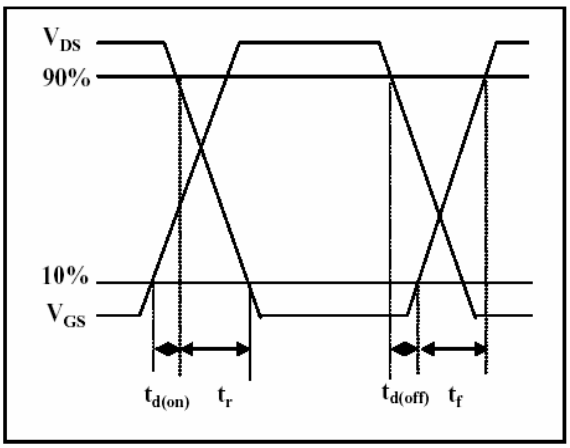


Fig 14. Switching Time Waveform

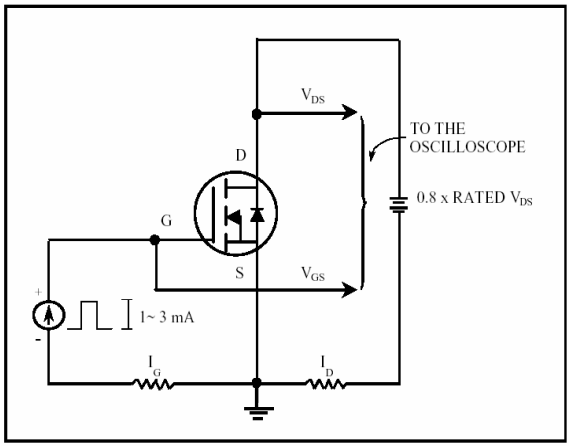


Fig 15. Gate Charge Circuit

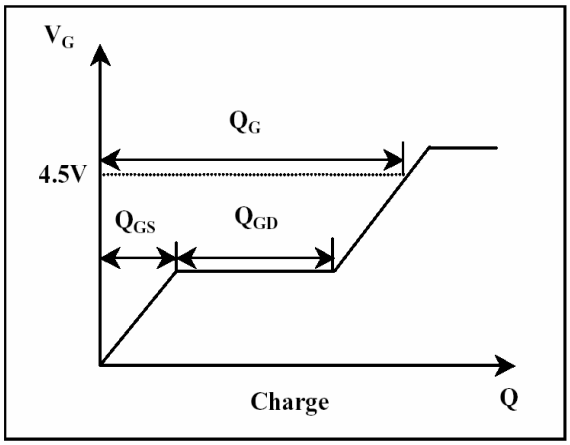


Fig 16. Gate Charge Waveform

P-Channel

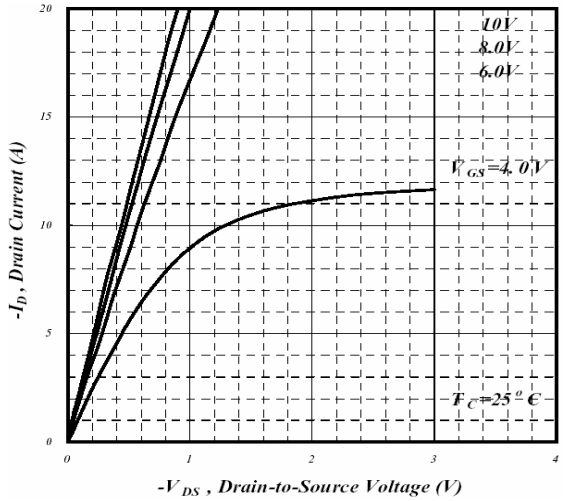


Fig 1. Typical Output Characteristics

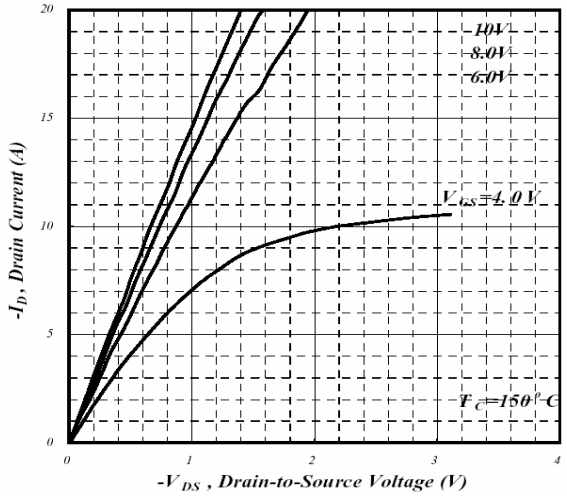


Fig 2. Typical Output Characteristics

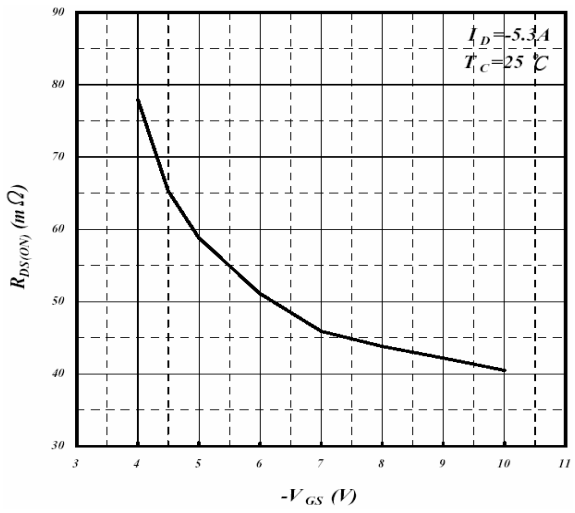


Fig 3. On-Resistance v.s. Gate Voltage

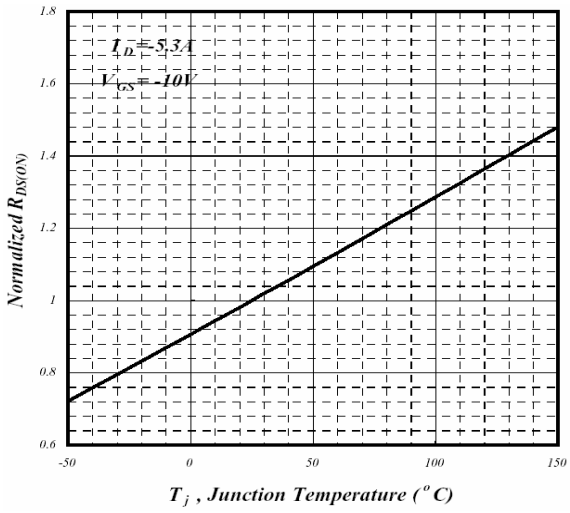


Fig 4. Normalized On-Resistance v.s. Junction Temperature

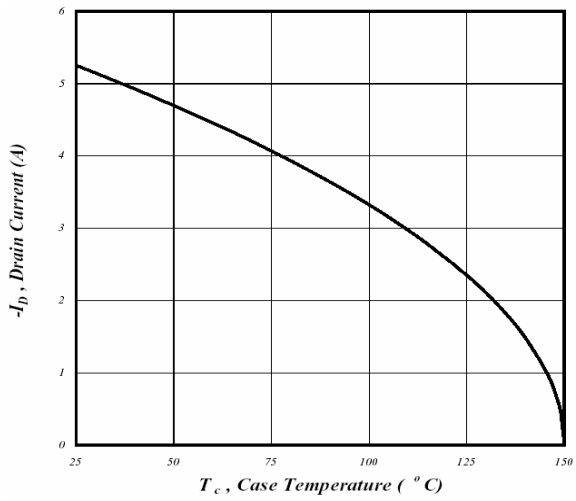


Fig 5. Maximum Drain Current v.s. Case Temperature

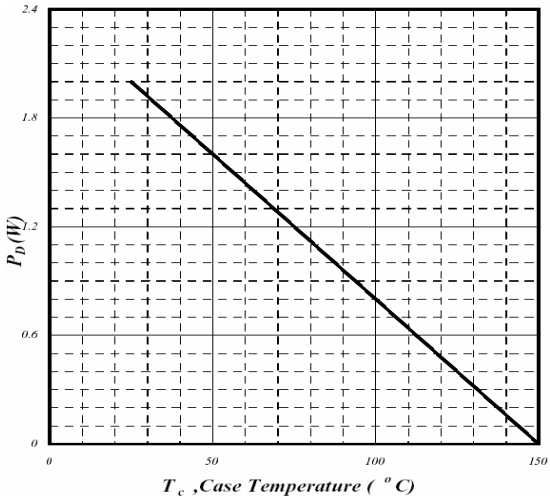


Fig 6. Type Power Dissipation

P-Channel

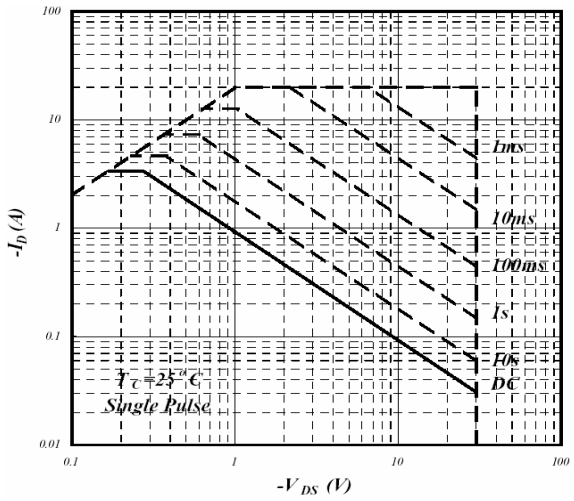


Fig 7. Maximum Safe Operating Area

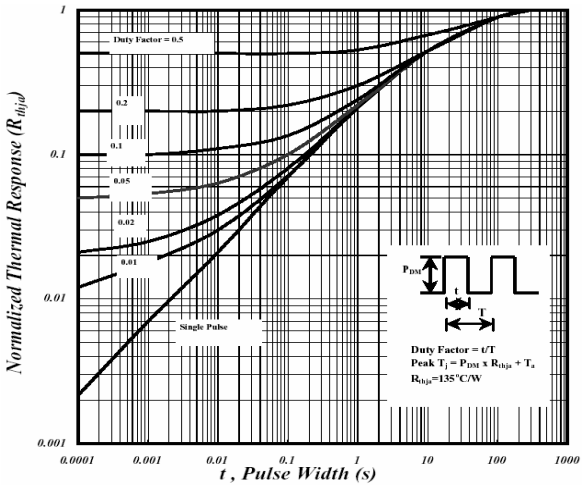


Fig 8. Effective Transient Thermal Impedance

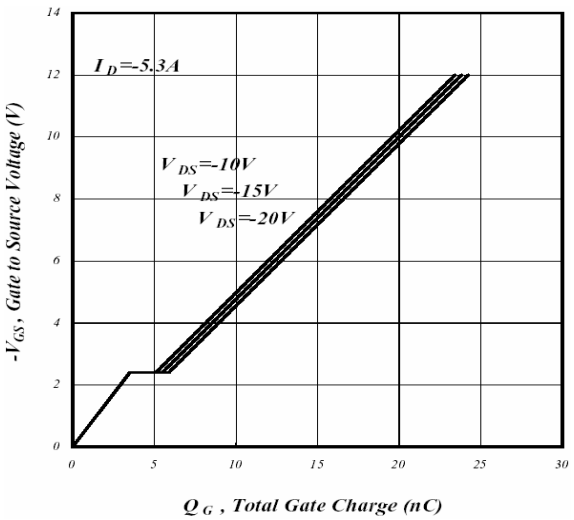


Fig 9. Gate Charge Characteristics

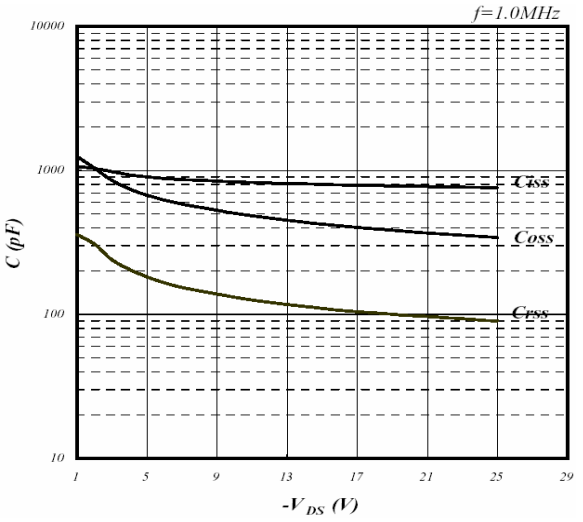


Fig 10. Typical Capacitance Characteristics

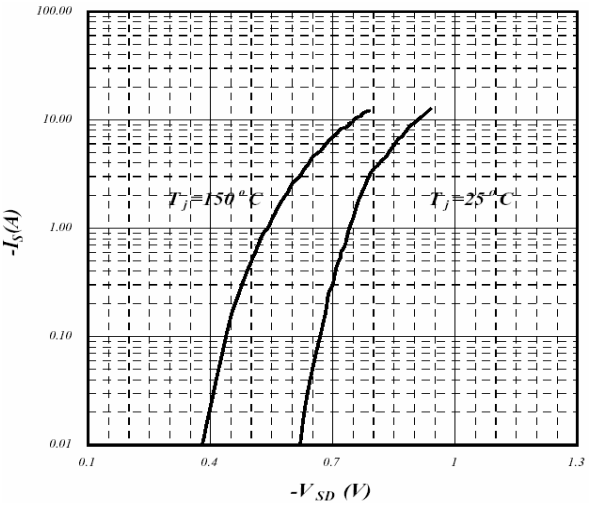


Fig 11. Forward Characteristics of Reverse Diode

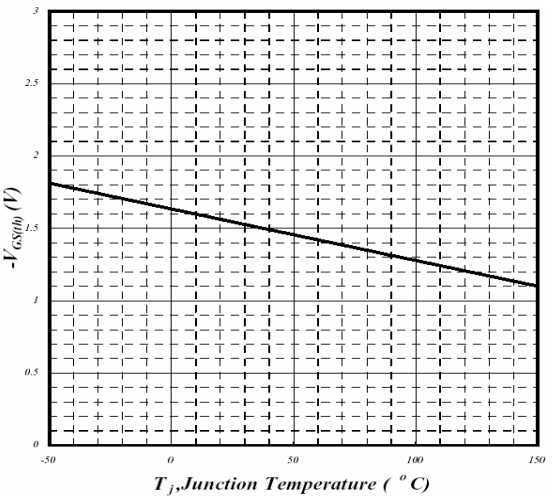


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

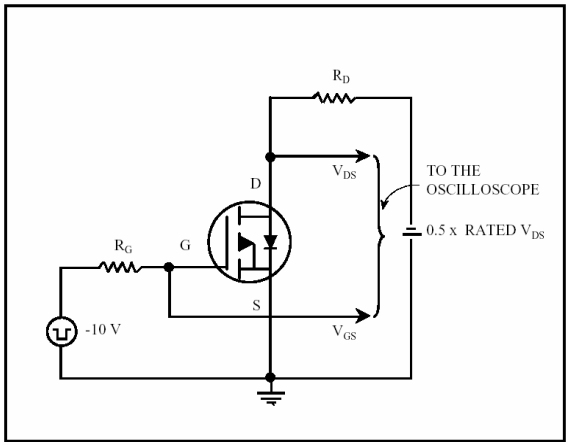


Fig 13. Switching Time Circuit

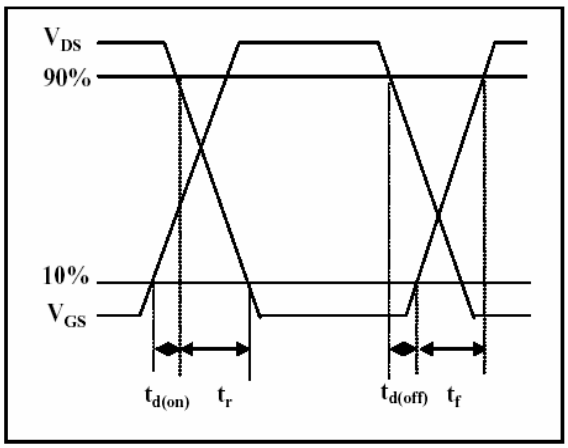


Fig 14. Switching Time Waveform

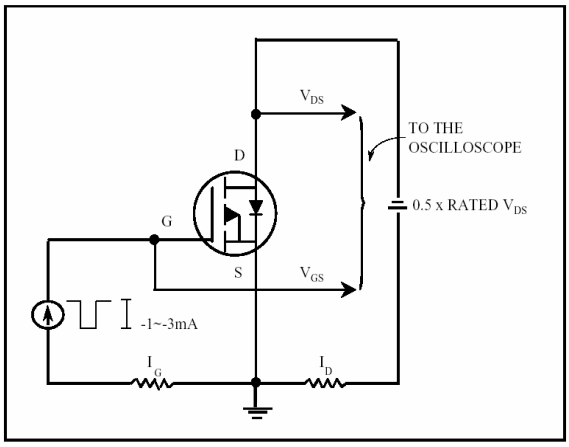


Fig 15. Gate Charge Circuit

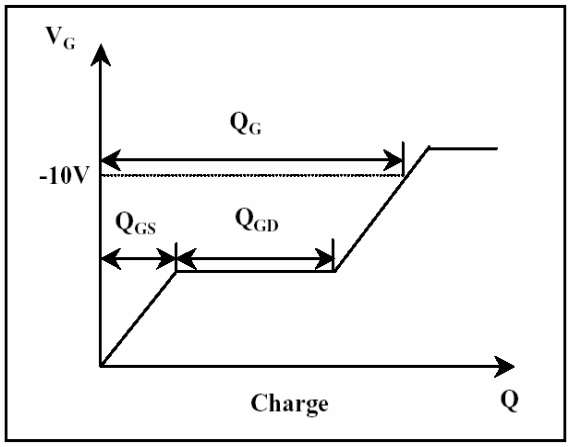


Fig 16. Gate Charge Waveform

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